REMARKS

The Office Action dated January 27, 2005 has been received and carefully considered. In this response, claims 7 and 41 have been amended to improve their form. Support for the amendments may be found in the specification and figures as originally filed and the amendments do not narrow the scope of the claims. Entry thereof and reconsideration of the outstanding rejections in the present application is respectfully requested in view of the following remarks.

Allowability of Claims 1-34

The Applicants note with appreciation the indication at page 2 of the Office Action that claims 1-34 are allowed.

Anticipation Rejection of Claims 35-41

Claims 35-41 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Artieri (U.S. Patent No. 6,104,751). This rejection is respectfully traversed with amendment.

Claim 35, from which claims 36-41 depend, recites the limitations of receiving a first client request from a first video decoder, routing the first client request to a first memory controller, receiving a second client request from a second video decoder, and routing the second client request to a second memory controller. The Examiner asserts that Artieri discloses these limitations. In particular, the Examiner asserts that Figure 3 of Artieri discloes an MPEG decoder having a memory controller (MCU) 24 "that serves to carry out, uon request of the FIFOs, transfer operations between these FIFOs and picture memory" and further asserts that Figure 8 of Artieri teaches four MPEG decoders, where "between each decoder, there is provided an exchange system allowing a decoder to provide the data of its slice to its memory and provide the same data to the memories of adjacent decoders through an exchange bus XBUS (col. 20, lines 59-67, and col. 21, lines 1-14)." *See Office Action*, p. 4.

As noted above, claim 35 recites that first and second client requests are received from first and second video decoders, respectively. Claim 35 further recites that the first and second

client requests are routed to first and second memory controllers, respectively. As asserted by the Examiner and as illustrated by Figures 3 and 6 of Artieri, each MPEG decoder of Figure 8 of Artieri includes an internal memory controller (MCU) 24. Further, Artieri teaches that the "client requests" are generated internally by the MPEG decoders and processed internally by the MCU 24 implemented as part of the MPEG decoder. Thus, no "client request" is output by the MPEG decoders of Figure 8 of Artieri, so Artieri fails to disclose that a "client request" is received from a video decoder as provided by claim 35. Consequently, Artieri necessarily fails to teach receiving first and second client requests from first and second video decoders and routing these first and second client requests to first and second memory controllers because Artieri teaches that memory controllers 24 are part of the MPEG decoder and therefore are not received from a video decoder and routed to a memory controller. Accordingly, it is respectfully submitted that Artieri fails to disclose each and every limitation of claim 35, as well as each and every limitation of claims 26-41 at least by virtue of their dependency from claim 35. Moreover, these claims recite additional limitations that are not disclosed by Artieri.

To illustrate, claim 38 recites the additional limitations of wherein a number of requests routed to a memory controller from a particular client is dependent on the data rate of the particular client. The Examiner asserts that Artieri "teaches the system includes a plurality of processing elements decoding parameters, and a memory bus controlled by a memory controller to exchange data between the processing elements at rates adapted to the processing rates of these elements, and to store in a picture memory data to be processed or re-used (col. 3, lines 40-49)." *Office Action*, pp. 4-5. For ease of reference, the cited passage of Artieri is reproduced below:

> The present invention more particularly addresses a system for processing compressed data arriving in packets corresponding to picture blocks, these packets being separated by headers containing decoding parameters of the packets. The system includes a plurality of processing elements using said decoding parameters, and a memory bus controlled by a memory controller *to exchange data between the processing elements at rates adapted to the processing rates of these elements*, and to store in a picture memory data to be processed or re-used.

Artieri, col. 3, lines 40-49 (emphasis added).

The Applicants note that the cited passage of Artieri teaches that a memory bus is

controlled by a memory controller to *exchange data between the processing elements at rates adapted to the processing rates of these elements. See Id.* However, the cited passage of Artieri makes no mention of data requests, nor does the cited passage disclose that the *number* of requests routed from a memory controller to a client is based on the data rate of the client. Accordingly, the Applicants respectfully submit that the Office Action fails to establish that Artieri discloses each and every limitation of claim 38.

In view of the foregoing, it is respectfully submitted that the anticipation rejection of claims 35-41 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Conclusion

It is respectfully submitted that the present application is in condition for allowance and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

27 April 2005
Date

Ryan S. Davidson, Reg. No. 51,596
On Behalf Of
J. Gustav Larson, Reg. No. 39,263
Attorney for Applicant
TOLER, LARSON & ABEL, L.L.P.
5000 Plaza On The Lake, Suite 265
Austin, Texas 78746
(512) 327-5515 (phone)
(512) 327-5452 (fax)